AMENDMENTS TO THE CLAIMS

Please cancel claim 8 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a processor configured to operate at a first data rate in response to a first clock signal;

an interface circuit having a state machine and configured to (i) operate at a second data rate in response to ~~the first~~ a second clock signal, and (ii) convert data received from said processor over a system bus from said first data rate to ~~a~~ said second data rate; and

a memory having a plurality of banks (i) coupled to said interface circuit and (ii) configured to present/receive data to/from said system bus at said second data rate, wherein said state machine is configured to precharge and close all of said plurality of banks prior to a refresh cycle being performed.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first clock signal and said second clock signal are independently generated.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second clock signal is generated in response to said first clock signal.

4. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein ~~said interface circuit comprises a~~ state machine is configured to control the conversion between said first and said second data rate.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said apparatus provides paging to said memory.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said processor comprises (i) a central processing unit (CPU) and a bus interface unit, wherein said CPU communicates with said system bus through said bus interface unit.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said interface further comprises a bus interface, wherein said state machine is configured to communicate with said system bus through said bus interface unit.

8. (CANCEL)

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said interface is configured to minimize access requests to said memory.

10. (CURRENTLY AMENDED) An apparatus comprising:

processor means for operating at a first data rate in response to a first clock signal;

interface means having a state machine for (i) operating at a second data rate in response to ~~the first~~ a second clock signal, and (ii) converting data received from said processor means over a system bus from said first data rate to ~~a~~ said second data rate; and

memory means having a plurality of banks for (i) coupling said interface means ~~circuit~~ and (ii) presenting data to/from said system bus at said second data rate, wherein said state machine is configured to precharge and close all of said plurality of banks prior to a refresh cycle being performed.

11. (CURRENTLY AMENDED) A method for paging to a memory comprising the steps of:

(A) operating a processor at a first data rate in response to a first clock signal;

(B) operating an interface circuit at a second data rate in response to a ~~first~~ second clock signal;

(C) converting data received from said processor over a system bus from said first data rate to ~~a~~ said second data rate; ~~and~~

(D) operating a memory having a plurality of banks coupled to said interface circuit and for presenting/receiving data to/from said system bus at said second data rate; and

(E) precharging and closing all of said plurality of banks prior to a refresh cycle being performed.

Please add the following new claims:

12. (NEW) The apparatus according to claim 1, wherein said processor includes a direct memory access engine and said apparatus provides a delay when said direct memory access engine is not ready to present/receive data to/from said memory during a read/write operation.

13. (NEW) The apparatus according to claim 12, wherein said interface circuit comprises a control status register having a completion bit which indicates that said apparatus is ready to begin a new read/write operation.

14. (NEW) The apparatus according to claim 13, wherein said apparatus is ready to begin a new read/write operation to/from said memory when said completion bit is cleared.

15. (NEW) The apparatus according to claim 14, wherein a direct memory access upper bound register is set in response to said completion bit being cleared.

16. (NEW) The apparatus according to claim 15, wherein a direct memory access lower bound register is set depending on whether said apparatus is performing the read/write operation to/from said memory.

17. (NEW) The apparatus according to claim 16, wherein said direct memory access engine is configured to perform (i) a write operation when said direct memory access lower bound register is clear and (ii) a read operation when said direct memory access lower bound register is set.

18. (NEW) The apparatus according to claim 17, wherein said direct memory access engine is configured to present an interrupt signal to said processor in response to completing a block of transfer during the read/write operation.

19. (NEW) The apparatus according to claim 18, wherein said processor is configured to determine if more blocks are needed to be transferred during the read/write operation.

20. (NEW) The apparatus according to claim 19, wherein said completion bit is set if there are no more blocks needed to be transferred during the read/write operation.

21. (NEW) The apparatus according to claim 13, wherein said control status register includes a direction bit configured to indicate (i) a write operation when said direction bit is clear and (ii) a read operation when said direction bit is set.